CLAIMS:

1. A down converter, comprising:
an integrated circuit having a control FET (CF) and a synchronous rectifier FET (SF), wherein the control FET is an LDMOS FET, and a conductivity-type of the LDMOS FET and a conductivity-type of a substrate are of the same type.

2. A down converter as recited in claim 1, wherein the synchronous rectifier FET is a VDMOS FET.

3. A down converter as recited in claim 1, wherein the synchronous rectifier FET is a vertical trench DMOS FET.

4. A down converter as recited in claim 1, wherein the synchronous rectifier FET is another LDMOS FET.

5. A down converter as recited in claim 2, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of a few milli-Ohms from a source of the control FET to an output on a surface of a substrate.

6. A down converter as recited in claim 3, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of a few milli-Ohms from a source of the control FET to an output on a surface of a substrate.

7. A down converter as recited in claim 4, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of a few milli-Ohms from a source of the control FET and a drain of the synchronous rectifier FET to an output on a surface of a substrate.

8. A down converter as recited in claim 2, wherein the VDMOS FET and the LDMOS FET are disposed in respective wells having opposite polarity.

9. A down converter as recited in claim 3, wherein the vertical trench DMOS FET and the LDMOS FET are disposed in respective wells having opposite polarity.

10. A down converter as recited in claim 1, wherein the integrated circuit does not include isolation regions between the CF and the SF.

11. A down converter as recited in claim 1, wherein the conductivity type is n-type.

12. A down converter, comprising an integrated circuit having a control FET (CF) and a synchronous rectifier FET (SF), wherein the control FET and the synchronous rectifier FET are each LDMOS FET's, and a conductivity-type of the LDMOS FET's and a conductivity of the substrate are of the same conductivity type.

13. A method of switching an electrical load, the method comprising:
providing a power-converter that includes an integrated circuit having a high-side switch and a low-side switch, wherein the high-side switch is an LDMOS FET, and the conductivity-type of the LDMOS FET and the conductivity of the substrate are of the same type.

14. A method as recited in claim 13, wherein the low-side switch is a VDMOS FET.

15. A method as recited in claim 13, wherein the low-side switch is a vertical trench DMOS FET.

16. A method as recited in claim 13, wherein low-side switch is another LDMOS FET.

17. A method as recited in claim 14, wherein the power converter further comprises a plurality of conductive plugs, which provide an ohmic connection of a few milli-Ohms to an output on a surface of a substrate.

18. A method as recited in claim 15, wherein the power converter further comprises a plurality of conductive plugs, which provide an ohmic connection of a few milli-Ohms to an output on a surface of a substrate.

19. A method as recited in claim 16, wherein the power converter further comprises a plurality of conductive plugs, which provide an ohmic connection of a few milli-Ohms to an output on a surface of a substrate.

20. A method as recited in claim 13, wherein the high side switch is a CF, and the low-side switch is an SF.